OIPE JC101 NOV 26 2004 PATENT & TRADEMARK OFFICE

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application Of:

Dvorak, et al.

Application No.: 09/981,603

Filed: November , 2004

For: Arc Fault Circuit Interrupter System

Atty. Docket No.: 47181-00259

Examiner: Boris Benenson

Group Art Unit: 2836

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to the Assistant Commissioner for Patents, Attn: Box Non-Fee Amendment, Washington, D.C. 20231, on:

Date: Nov 23, 2004

Signature: Christina Rozell

37 C.F.R. § 1.131 DECLARATION OF KON B. WONG

Assistant Commissioner for Patents
Alexandria, VA 22313-1450

Attn: Box Non-Fee Amendment

I, KON B. WONG declare:

1. I am a co-inventor, with Robert F. Dvorak, of the subject matter described and claimed in the above-identified patent application, Application No. 09/981,603 ("the present application").

2. This declaration is to establish completion of the invention in the present application in the United States, at a date prior to July 10, 2001, the effective date of U.S. Patent No. 6,259,996, which was cited by the Examiner.

3. The document attached hereto as Exhibit 1 is a true photocopy of an invention disclosure statement dated prior to July 10, 2001 (date redacted) showing completion of the above-identified application in the United States of America prior to July 10, 2001.

4. Robert F. Dvorak and I diligently worked on the arc fault circuit interrupter system from at least a time prior to July 10, 2001 until the completion of the filing date of the present application. Our work during this time period included the actual work on the subject device as well as coordinating with the attorneys to prepare the patent application.

5. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the above-referenced application or any patent issuing thereon.

November 22, 2004
DATE

Kon B. Wong
KON B. WONG

To be completed by Law Dept.

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CONFIDENTIAL AND PROPRIETARY PROPERTY TO [redacted]

RETURN TO LAW DEPT. WHEN COMPLETED

REDACTED

Invention Disclosure for Patent Application

Dedicated to Growth • Committed to Quality

DATE SUBMITTED:

INSTRUCTIONS:
Inventors must fill in all items 1 to 22. Items 2, 3 and others may require extra sheets. Be sure they are signed, witnessed and attached.

1. Name of the Invention. (Limit to ten words).
Arc Fault Circuit Interrupter System on Chip

2. What are the problems solved by this Invention? (Use separate sheets if necessary.)

Residential type circuit breakers incorporating arc fault circuit protection require a very small printed wiring board with low power dissipation. Arc fault circuit interruption requires significant analog and digital signal processing in order to reliably distinguish between arc faults and electrically noisy loads, such as arcs from light switches and universal motors. In a previous embodiment, such processing was achieved using a separate analog ASIC (application specific integrated circuit) and a microcontroller. A more cost effective solution is required to maintain a competitive position in the market place. Combining as much functionality as possible on a single microchip minimizes space and lowers part cost. Furthermore, by driving more of the previously required external components onto the chip, the associated part and assembly costs can be eliminated.

3. Give a complete description of the Invention, including its operation, purpose and environment. (Use separate sheets if necessary.)

See attached sheets

4. What improvement over the known technology (technologies of Square D and Others) is accomplished by this Invention?

The system on chip design provides a reduced package size, approximately 1/3 reduction, as well as a reduction in external components required. The combination of reduced parts and part placement results in a significant cost reduction and ease of assembly. Bandpass filter performance is more consistent, offset voltage correction is improved, test circuit performance is improved, and ground fault personnel protection can be provided.

5. List the closest known technology (e.g. publication, patent or commercial products of Square D or others) providing the same or similar results?

Square D AFCI modules in HOM and QO circuit breakers.

6. What new elements (e.g. components, circuits, process steps) or new combinations of known elements or software algorithm produced the improvement?

a. The combination of the analog and digital processing in a single chip, that is system on chip
b. Use of 0.5 micron CMOS technology
c. A three channel MUX combined with a single channel A/D converter
d. Switched capacitor bandpass filters
e. Two stage ground fault amplification
f. A current source driven test buffer
g. On chip voltage regulator
h. A clock gated ANDing of the bandpass filter comparator outputs
i. Offset measurement and software correction.

7. What are the potential applications for use of this invention?
QO and HOM 15 and 20 ampere circuit breakers with arc fault detection.

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8. What was the mental conception date of this Invention? (Attach pertinent engineering log sheets, drawings, etc., to support dates. Always attach the earliest drawing and the earliest written description.)

9. To whom did you first disclose this invention?

Name Andy Haun

10. When was the device first built and tested? REDACTED

DETERMINATION OF LEGAL INVENTORSHIP FOR PATENT APPLICATION MUST BE MADE BY PATENT COUNSEL.

11. Have you previously seen or heard of this Invention (or a similar invention)? If so, please explain structural differences from your invention.

NO

12. When (was) (will) the first offer for sale of a product incorporating this Invention (be) made? REDACTED

13. When (was) (will) the first disclosure outside Square D (be) made? How and to whom? State title and date of publication, if any.

Unknown

14. Who are the potential competitors?

GE
Eaton
Siemens

15. Did this Invention result from work on a Government Development or third party's Contract? Yes ☐ No X

16. List any additional persons (excluding those listed as Inventors on page 4) who contributed to the Invention.

Inventor's signature. IMPORTANT: You must use your full name – no initials.

17. Inventor's Name (Type) Kon Bing Wong

Signature Kon Bing Wong

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Witness' signatures. TWO WITNESSES ARE REQUIRED. Witness must sign this form and all attachments hereto.

IN SIGNING THIS FORM THE WITNESSES ATTEST TO THE FACT THAT THEY UNDERSTAND THE INVENTION.

21. Witness Name: (Type) Henry J. Zylstra

Signature Henry J. Zylstra

REDACTED

22. Witness Name: (Type) Paul A. Reid

Signature Paul A. Reid

Description of the Invention:

This invention pertains to the use of a Sytem on Chip solution for arc fault detection primarily for use in circuit breakers or receptacles, typically but not limited to the 15 or 20 ampere size. This microchip, when incorporated on an electronic printed wiring board with a minimum of external components, provides arc fault detection and tripping of the host wiring device.

The system on chip is an application specific integrated circuit which combines analog and digital signal processing on a single microchip. A block diagram is shown in Figure 1 below.

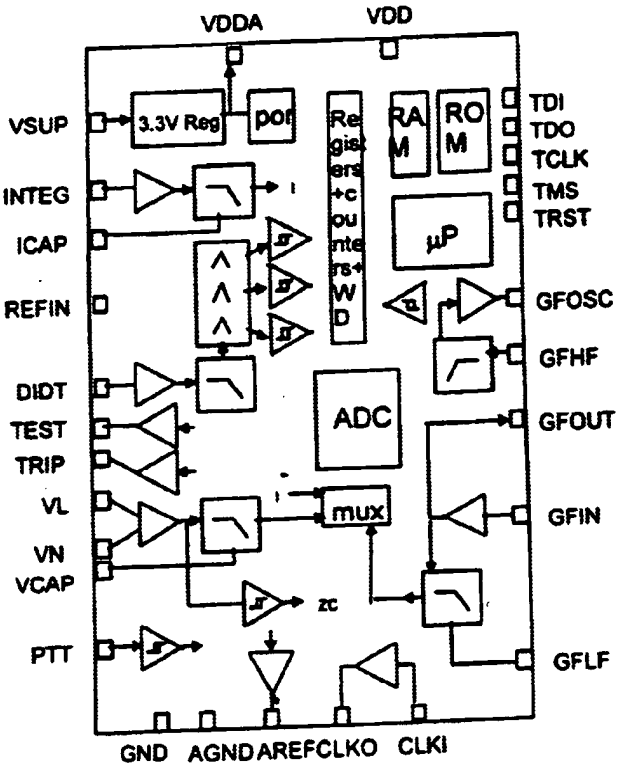

Figure 1

The system on chip monitors line voltage and current in the host device and analyzes them for the presence of an arc fault. If certain arc detection criteria are met as determined by an arcing algorithm embedded within the software of the microcontroller's memory, the chip signals an external firing circuit causing it to disconnect the device from the load.

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The various functional blocks and their respective operation is described below.

a. 3.3V Reg
The 3.3V regulator provides a finely regulated DC power source for use by the analog and digital sections of the chip. The input to the chip need only be roughly regulated to within course limits, for example 4 to 7 volts.

b. POR
The POR or power on reset circuit senses the chips regulated voltage supply and holds the microcontroller in a reset state if the voltage is below a safe operating limit.

c. AREF
The analog reference circuit provides a reference point for the input signals at the midpoint of the analog power supply to allow the amplified signals to swing both positive and negative. The AREF is externally connected to the REFIN pin.

d. Vl/Vn
This circuit differentially measures line voltage at the terminals of the host device via an externally located voltage divider. The voltage signal is low pass filtered as shown at the low pass filter block to remove high frequency noise or harmonics and to provide anti-aliasing. The filtered signal is sent to a first channel of a multiplexer and also to the input of a zero crossing detector.

e. ZC
A comparator at the output of the line voltage differential amplifier detects zero crossings in the line voltage for use in synchronizing the arc detection algorithm.

f. INTEG
The amplifier at the INTEG input amplifies the externally integrated output of a di/dt sensor before it is lowpass filtered for anti-aliasing and sent to a second channel of the multiplexer previously referenced.

g. DIDT
The output of a di/dt sensor monitoring line current through the host device is connected to the input of the DIDT amplifier after first being high pass filtered to remove the 60 Hz component. The di/dt signal is amplified and sent to the input of three bandpass filters. Broadband noise in the 10KHz to 100KHz range appearing at the DIDT input is one indicator of the presence of arcing.

h. Bandpass Filters
Figure 2 shows a more detailed block diagram of the di/dt sensing system.Three switched cap bandpass filters set at 20, 33 and 58 Khz filter the di/dt signal to determine if there is broadband noise in the line current. The 20 KHz filter is provided for added flexibility in future arc detection devices. The output of the filters is monitored by a set of comparators whose outputs change state when a predetermined threshold is exceded. The microprocessor monitors the state of each filter's comparator individually and also the logically ANDed output of the 33 and 58 KHz filters to determine the presence of a more broadband noise than that of either of the filter's bandwidths. The comparator output and the AND gates are synchronized by the clock of the switched capacitor bandpass filters. It should be noted that the

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ANDing of the comparator outputs with the clock insures that the components of high frequency in the passbands of both the 33KHz and 58KHz filters must be simultaneously present and of sufficient amplitude in order to be considered broadband noise and therefore be counted by the 33/58 counter.

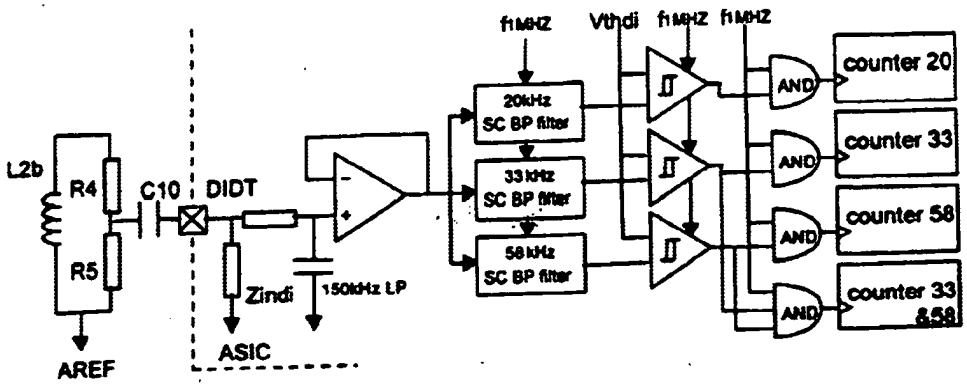

Figure 2

i. **GFIN**
The output of a ground fault sensing transformer is connected to the input of the GFIN amplifier, which has a high gain to amplify the small output from the sensor.The ground fault signal is amplified and lowpass filtered for anti-aliasing before being fed to the third channel of the multiplexer.

j.**GFHF**
The chip has provision for personnel level ground fault protection when provided with a 5 mA ground sensing transformer and a second neutral detecting transformer. To make this feature functional, the output of the GFOUT is coupled by means of a capacitor to the input of GFHF. GFOSC is then capacitively coupled to the winding of a neutral sensing transformer. When thus connected, this forms a dormant oscillator neutral detection system. The function of the second amplifier at GFHF is to provide the total loop gain necessary to put the dormant oscillator into oscillation when a sufficiently low resistance grounded neutral condition exists.

k. **MUX**
The multiplexer alternately selects between the three channel inputs, ie current, line voltage or ground fault and passes the selected signal to the input of the A/D converter.

l. **ADC**
The analog to digital converter is a single channel sigma delta converter which alternately ditizes the current, line voltage and ground fault signals for analysis by the microprocessor.

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m. **Microprocessor**
The processor is an ARM7MTDI from the ARM company. It is 32 bit wide and has a cpu frequency of 4 Mhz in the present embodiment. An external resonator has a frequency of 8 MHz which is divided by two for the cpu. The microprocessor analyzes the current, ground fault and di/dt signals and by means of an arc detection algorithm makes a trip decision. While the line voltage is fed to the microprocessor, it may be optionally used by the algorithm to effect various levels of arc detection as dictated by the embedded software. The microprocessor uses the zero crossing signal to synchronize the arc detection algorithm with line voltage.

n. **RAM/ROM**
There are two memories. The program ROM contains the software for the ARM operation and is a 10KB(2560 words of 32 bits). The data memory contains the program data and consists of two RAMs of 128 bytes x 16 bits for a total of 512 bytes.

o. **W/D**
The watchdog monitors the operation of the ARM microprocessor. If the software does not reset the watchdog counter between 65 and 131 milliseconds, the watchdog generates a hard reset of the microprocessor. Alternately, it could be used to cause a trip condition.

p. **JTAG Interface**
The ARM has a communication channel used for production test. It is accessible by pins TDI, TDO, TMS, TCK and TRST.

q. **TRIP**
When a trip decision is reached, the trip signal buffer latches and drives the gate of an SCR of an external firing circuit. In order to conserve stored energy during the trip sequence, the microprocessor is halted and portions of the analog circuitry are disabled. The SCR is connected in series with a trip coil. In the ON state, the SCR causes the coil to be momentarily shorted across the line to mechanically de-latch the contacts of the host device and to subsequently interrupt flow of current.

r. **PTT**
The push to test circuit monitors the status of the push to test button. When the push to test button is depressed, line voltage is applied through an external voltage divider circuit to the PTT circuit. The circuit senses that a system test is being requested and signals the microprocessor to enter a test mode.

s. **TEST**
With the microprocessor in the test mode, the test signal buffer acts as a current source driving the test winding of the di/dt sensor with a sharply rising and falling edge square wave at each of the center frequencies of the bandpass filters, namely 20 KHz(when used), 33 KHz and 58 KHz in turn.

Additional Operational Description:
The ground fault detection feature's primary purpose is to detect arcing to ground,in the incipient stages of arcing, where a grounding conductor is in the proximity of the faulty line conductor. Such detection and tripping can clear arc faults before they develop into major events. As discussed earlier, by the use of appropriate ground fault and neutral sensing

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transformers, this feature can be used to provide personnel protection as well as arc to ground detection.

In the push to test mode, the push to test button in the host device forces a test ground fault current to flow through the ground fault sensing transformer and simultaneously forces the microcontroller into the test mode as described previously. The microprocessor monitors the output of both the ground fault detection circuitry and the output of the bandpass filters (caused by the test buffer driving the test winding) to determine if the detection circuitry is fuctional. Only if all signals are present will a trip signal be given signifying the test passed.

A calibration routine allows the microprocessor to compensate for the offset voltages generated by the operational amplifiers in the line voltage, current and ground fault measurement circuits. Immediately following power up and at periodic intervals, the microprocessor iniates a calibration procedure. During this time period, the line voltage and current measurement circuits are internally disconnected from their respective input terminals and the amplifiers connected to the analog reference voltage. The offset voltages are then read by the microprocessor and their values are stored in memory. The stored offset voltages are subtracted from the measured signal values by the software. The ground fault offset is measured by internally shorting the first stage amplifier gain setting resistors and reading the offset voltage on the external AC coupling capacitor directly from the input. In the previosly described manner, the software subtracts this value from the measured signal value.

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